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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/084,341 | 02/28/2002 | Takashi Suzuki | 046124-5115 | 5600 |

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| EXAMINER | |
|---|---|
| PATEL, GAUTAM | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2655 | |

DATE MAILED: 05/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/084,341 | SUZUKI ET AL. | |
| | Examiner | Art Unit | |
| | Gautam R. Patel | 2655 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-25-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## Response to Amendment

1. This is in response to amendment filed on 2-28-05

2. claims 1-3 remain for examination.

## Claim Rejections - 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 & 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by et al., US. patent 5,822,346 (hereafter Arai).

As to claim 1, Arai discloses the invention as claimed; a drive current supply circuit [see Figs. 1] including a first current mirror circuit, and a control circuit, comprising:

a first current mirror circuit [fig. 1, unit 14, 15, & 11] having two parallel lines [output of 10 or 11] & output of 14, 15 and 16], said laser diode [fig. 1, unit 1] being connected with one [line from unit 14] of the two parallel lines; and

a control circuit [fig. 1, unit 4, & especially 10, 11, 12 and 13] connected with the other of the two parallel lines, said control circuit controlling the current flowing in this line in accordance with a potential of this line, this potential comprising a steady DC component [read power current Ir] when reading data; and this potential comprising a drive signal component added [fig. 1, output of 10 to 13 are added] to said DC component when writing data [col. 5, line 35 to col. 6, line 63].

4. The aforementioned claim 3, recites the following elements, inter alia, disclosed in Arai:

a second current mirror circuit [fig. 1, unit 16 & 12] having two parallel lines [output of 15], one of said lines of said second current mirror circuit being connected with said laser diode,

wherein said control circuit controls the current flowing through the other of said lines of said second current mirror circuit in accordance with a potential of the other of said lines, this potential comprising a steady DC component when reading data [Ir]; and this potential comprising a drive signal component added to said DC component when writing data [col. 5, line 35 to col. 6, line 63].

**Claim Rejections - 35 U.S.C. § 103**

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arai as applied to claims 1 and 3 above.

As to claim 2 Arai teaches all of the above elements including DC component for read mode and combination of AC and DC for write mode and several current mirror circuits. Ari does not teach the well know details of the construction of these mirror current sources such as that they are made up of field-effect transistors.

"Official Notice" is taken and maintained that both the concept and the advantages of providing field-effect transistors for construction of the current mirror are well known and expected in the art. It would have been obvious to include field-effect transistors to Ari's design as these field-effect transistors are known to provide high switching speed and are easy to construct on an integrated device. These concepts are very well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

NOTE: Arai was cited as prior art reference in previous paper.

6. Applicant's arguments filed on2-28-05 have been fully considered but they are not deemed to be persuasive for the following reasons.

7. In the REMARKS, the Applicant argues as follows:

A) That: "Applicants strenuously submit that, contrary to these assertions, Ari neither discloses nor suggests a current mirror circuit configured in the manner required by independent claim 1 and its dependent claims 2 and 3. A current mirror circuit, as can be understood with reference to, for example, the URL http://en.wikipedia.org/wiki/current_mirror ....(printout of page from URL enclosed), includes a pair of transistors, with gate (or base) of each transistor being connected to the gate (or base) of the transistor. Consequently, circuit elements 10, 11, 14, 15, and 16 do not [original emphasis] constitute such a current mirror structure. For example, element 14 of Arai relates to a current constant circuit, [original emphasis] controlled by D/A converter, whereas a current mirror circuit provides mirror currents in two lines." [page 6, para. 2; REMARKS].

FIRST: There may be a problem of semantics here. So lets first define what "current mirror" circuit is. This is circuit which provides [sources or sinks] constant current. This is done by supplying a reference current [first line] and supply or sink current [second line]. This is definition of current source or so called current mirror. To supply **constant current** one MUST have to have two transistors, one for reference one for supply.

SECOND: Yes, Arai has not shown well known details of constant current source. However one of ordinary skill in the art knows that when constant current is supplied [which Arai is doing; see col. 5, line 42; and this fact is admitted by the Applicants] it MUST have two transistors for constant current supply to work. So by definition Arai has two transistors. Also Arai shows a very well known international symbol for these kind of current sources [see attached documents].

THIRD: The URL link mentioned above is considered. The Applicants have stated that they have supplied these papers but these were not found with present amendment. However to expedite matters the Examiner has printed these papers out from the link. The very two lines on that papers state that "A current mirror is a circuit designed to regulate a current, to keep it constant regardless of loading".

In other words, according the definition supplied by the Applicants themselves defines that "constant current source" and "current mirror" are one and the same thing. Now since Arai is supplying constant current and shows them with international symbol for constant current and describes in detail that this a constant current source by definition he has a current mirror in units 14, 15, 16 and 17.

B) That: "Applicants also wish to point out that Applicants do not necessary agree with the Official Notice taken by the Examiner in the pending Office Action.

Examiner would like to point out that Kimura, US 6,516,015 was sent as other art. Kimura very clearly and exactly shows a current mirror designed form N-channel and P-channel field effect transistors on the face of the patent and also details inside. This current source is also designed for driving current through laser driver as claimed and disclosed in specification.

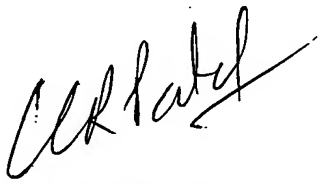
8. **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**Contact information**

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is 571-272-7625. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.
The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is 703-872-9306.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ms. Doris To can be reached on (571) 272-7629.
Any inquiry of a general nature or relating to the status of this application should be directed to the Electronic Business Center whose telephone number is 866-217-9197 or the USPTO contact Center telephone number is (800) PTO-9199.



GAUTAM R. PATEL
PRIMARY EXAMINER

Gautam R. Patel
Primary Examiner
Group Art Unit 2655

May 20, 2005